EAQD400-xxx-OM3

400Gb/s QSFPDD TO QSFPDD Active Optical Cable

PRODUCT FEATURES

- Hot-pluggable QSFP-DD form factor
- Case temperature range of 0℃to +70℃
- +3.3V single power supply
- Power dissipation < 10W per terminal
- Operating case temp
- 8x50G PAM4 retimed 400GUAI-8
- electrical interface aligned with IEEE 802.3bs
- Transmission distance up to 100m
- RoHS compliant

APPLICATIONS

- 200GAUI-4
- Other 400G optical links

DESCRIPTIONS

This is an MSA and TAA compliant 400GBase-AOC QSFP-DD to QSFP-DD active optical cable that operates over multi-mode fiber with a maximum reach of 1.0m (3.3ft). At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Active optical cables are RoHS compliant and lead-free.

Ordering Information

Part No.	
EAQD400-xxx-OM3	400G QSFP-DD to QSFPDD Active Optical Cable OM3 0~100M

Note:

1. where "x" denotes cable length in meters. Examples are as follows:
x = 1 for 1m, xx=10 for 10m

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc_3	-0.5	-	+3.6	V	
Storage Temperature	T_s	-10	-	+70	°C	
Operating Humidity	RH	+5	-	+85	%	1

Note:

1. No condensation

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	Pd	-	-	10	W	1
Bit Rate	BR	-	26.5625	-	GBaud	2

Note:

1. Per terminal

2. Per channel, PAM4

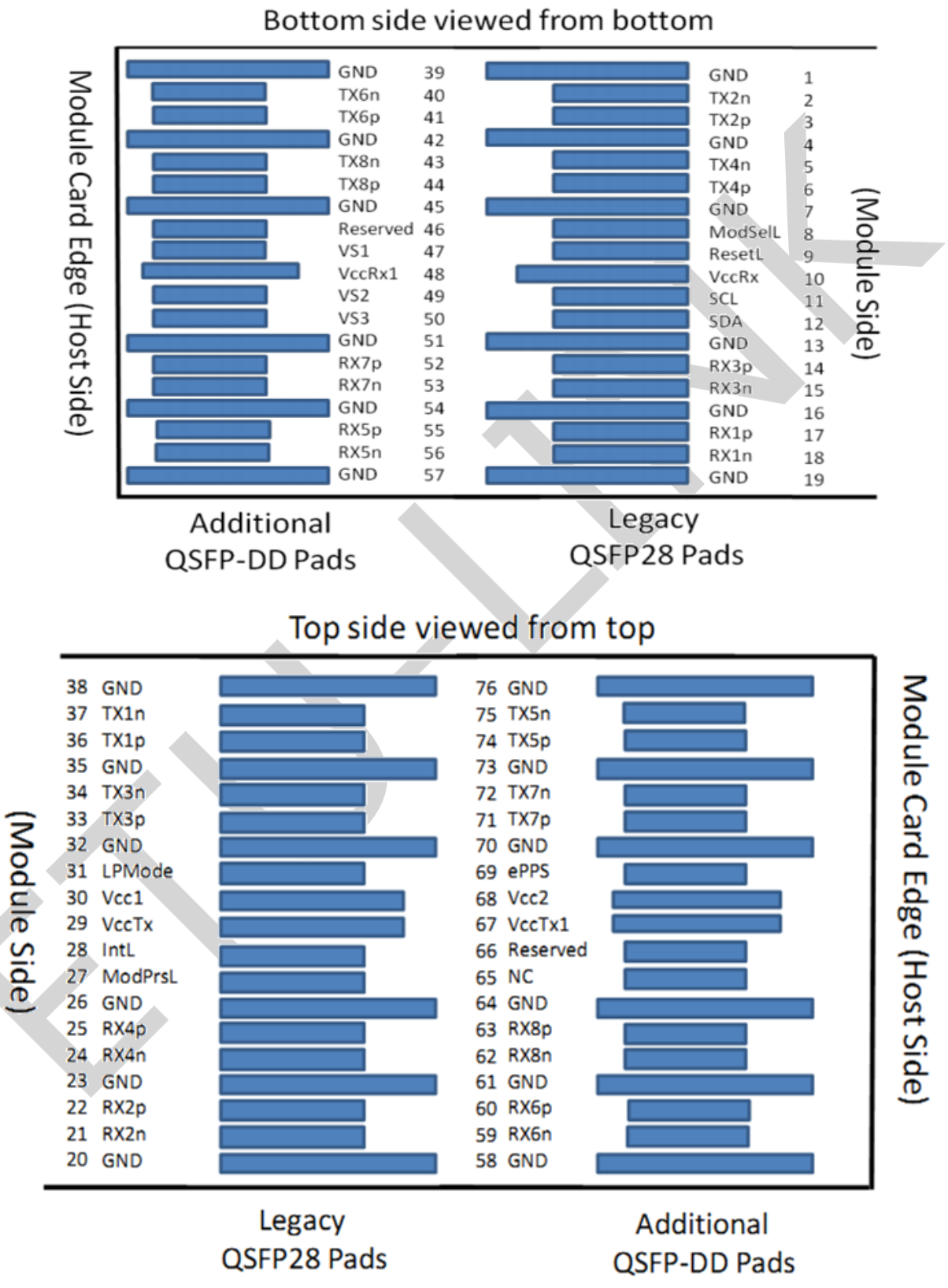
Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBaud	26.5625 ± 100 ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	900	-	-	
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBaud	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Near-end ESMW (Eye symmetry mask width)	-	UI	0.265	-	-	
Near-end Eye height, differential (min)	-	mV	70	-	-	
Far-end ESMW (Eye symmetry mask width)	-	UI	0.2	-	-	
Far-end Eye height, differential (min)	-	mV	30	-	-	
Differential termination mismatch	-	%	-	-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	
Bit Error Ratio	-	-	-	-	2.4E-4	1

Note:

1. Pattern PRBS31Q

Pin Diagram


Bottom side viewed from bottom
Module Card Edge (Host Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModSelL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19
(Module Side)
Additional QSFP-DD Pads
Legacy QSFP28 Pads
Top side viewed from top
(Module Side)
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 LPMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 ePPS
68 Vcc2
67 VccTx1
66 Reserved
65 NC
64 GND
63 RX8p
62 RX8n
61 GND
60 RX6p
59 RX6n
58 GND
Module Card Edge (Host Side)
Legacy QSFP28 Pads
Additional QSFP-DD Pads

Pin Definitions

Function Definitions for QSFP-DD

Pin	Name	Logic	Description	Power Seq	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	

32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reseved		For future use	3A	3

67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B

will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B

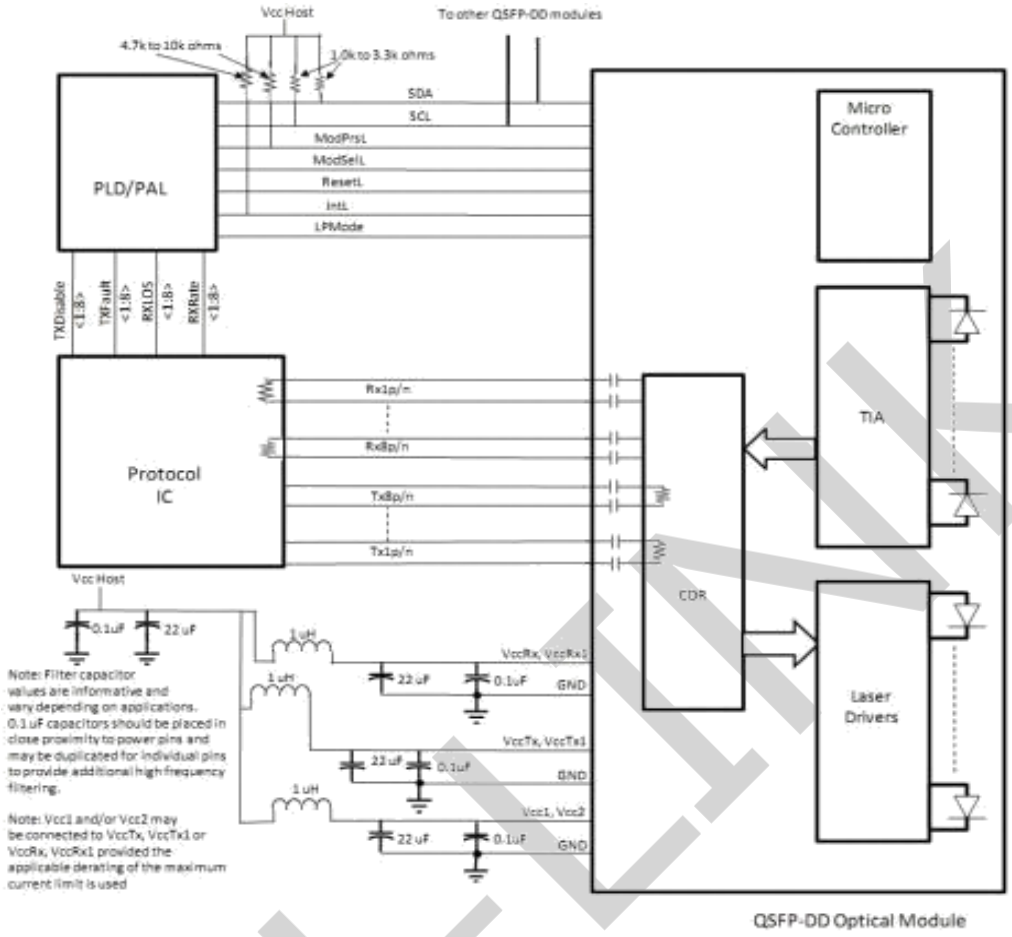
Note:

1. Circuit ground is internally isolated from chassis ground.

Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

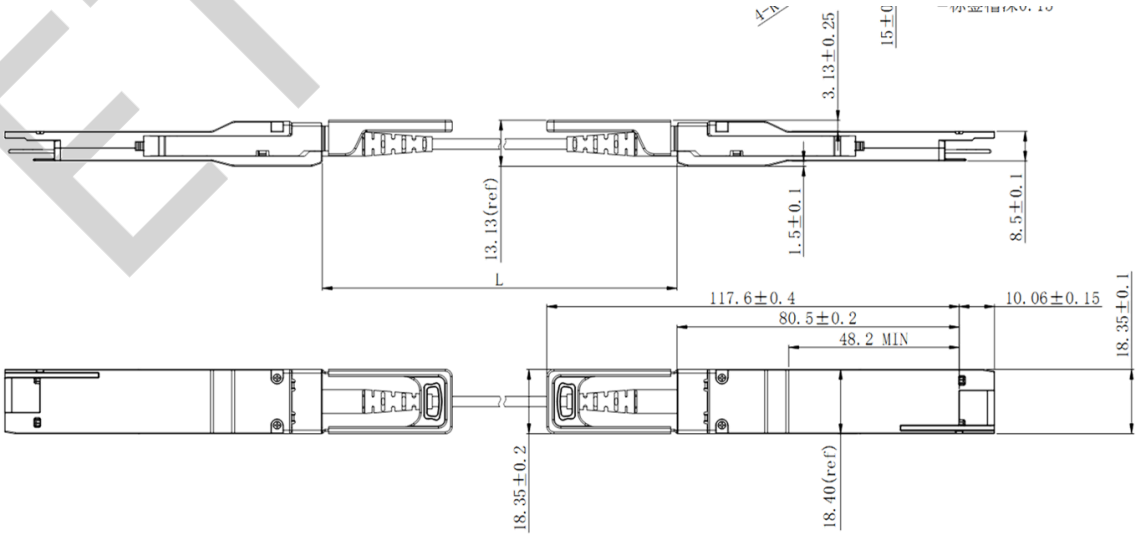
Recommended Interface Circuit



Mechanical Diagram

QSFP-DD AOC terminal are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

Unit mm



Cable Length

Cable Length（Unit: m）	Tolerant（Unit: cm）
< 1.0	+5/-0
1.0~4.5	+15/-0
5.0~14.5	+30/-0
≥15.0	+2%/-0

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.
Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

Revision History

Version No.	Date	Description
1.0	February 18, 2023	Preliminary datasheet
2.0	Aug 12,2024	Format change

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