

ESP852X-01DI

25Gb/s SFP28 100m DDM Transceiver

PRODUCT FEATURES

- Supports up to 25.78Gbps bit rates
- Hot-pluggable SFP+ footprint
- 850nm VCSEL laser and PIN photodiode
- 100m over M5F MMF (50/125 um OM4)
- 70m over M5E MMF (50/125um OM3)
- 20m on MMF (50/125um OM2)
- Compliant with SFP+ MSA and SFF-8472 with duplex LC receptacle
- Compatible with RoHS
- Single +3.3V power supply
- Real Time Digital Diagnostic Monitoring
- Operating case temperature:
Industrial: -40 to +85°C



APPLICATIONS

- 25GBASE-SR Ethernet
- CPRI option 10, 7, 8
- 100GE SR fan out to 4x25GE SR

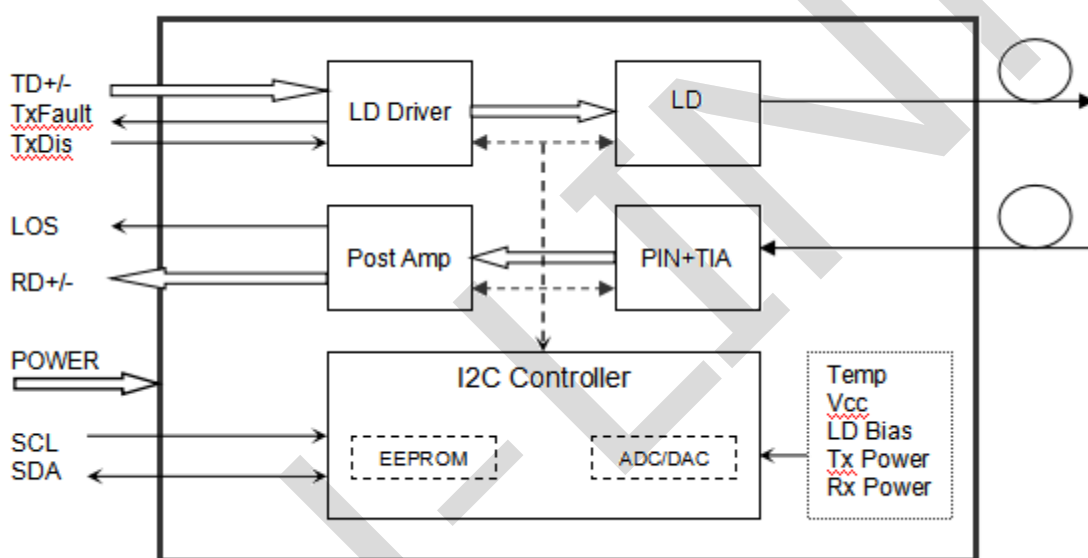
DESCRIPTIONS

The SFP28 transceivers are high performance, cost effective modules supporting data rate of 25.78Gbps over multimode fiber.

The transceiver consists of three sections: a VCSEL laser transmitter, a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and MCU control unit. All modules satisfy class I laser safety requirements.

The transceivers are compatible with SFP Multi-Source Agreement and SFF-8472 digital diagnostics functions.

Block Diagram



Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	Latch Color
ESP852X-01DI	25.78Gbps	VCSEL	MMF	100m	LC	-40°C~+85°C	Y	Black

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Ts	-40		+85	°C	
Operating Humidity	-	5		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _c	-40		+85	°C	
Power Supply Voltage	V _{cc}	3.135	3.30	3.465	V	
Power Supply Current	I _{cc}			300	mA	
Data Rate			25.75 10.3		Gbps	

Electrical Characteristics

High-Speed Signal: Compliant to CEI-25G-VSR

Low-Speed Signal: Compliant to SFF-8419

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter (Module Input)						
Differential Input Resistance	R _{Rdin}	90	100	110	Ω	
Input Differential Voltage	R _{Vdiff}	-	-	900	mVpp	
Tx_Disable	Normal Operation	V _{IL}	-0.3	-	0.8	V
	Laser Disable	V _{IH}	2.0	-	V _{CC} +0.3	V
Receiver (Module Output)						
Differential Resistance	T _{Rd}	90	100	110	Ohm	
Output Differential Voltage	T _{Vdiff}	-	-	900	mVpp	
Differential Termination Resistance Mismatch	T _{Rdm}	-	-	10	%	
Rx los	Normal Operation	V _{OL}	-0.3	-	0.4	V
	Loss Signal	V _{OH}	2		V _{CC} HOST	V

Optical and Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ _c	840	850	860	nm	
Spectral Width (RMS)	Δλ			0.6	nm	
Side-Mode Suppression Ratio	SMSR	-	-	-	dB	
Average Output Power @25.78Gbps and @10.3Gbps	P _{out}	-8.4		2.4	dBm	1
Extinction Ratio	ER	2.0			dB	
Data Input Swing Differential	V _{IN}	180		950	mV	2
Input Differential Impedance	Z _{IN}	90	100	110	Ω	
TX Disable	Disable		2.0		V _{cc}	V
	Enable		0		0.8	V
TX Fault	Fault		2.0		V _{cc}	V

	Normal		0		0.8	V	
Receiver							
Centre Wavelength	λ_c	840	850	860	nm		
Receiver Sensitivity@25.78Gbps				-8.6	dBm		3
Receiver Sensitivity@10.3Gbps				-11.1	dBm		4
Receiver Overload		2.4			dBm		3
LOS De-Assert	LOS _D			-13	dBm		
LOS Assert	LOS _A	-30			dBm		
LOS Hysteresis		0.5		4	dB		
Data Output Swing Differential	V _{out}	500		900	mV		5
LOS	High	2.0		V _{cc}	V		
	Low			0.8	V		

Notes:

1. The optical power is launched into MMF.
2. PECL input, internally AC-coupled and terminated.
3. Measured with a PRBS 2³¹-1 test pattern @25.78Gbps, BER ≤5E-5..
4. Measured with a PRBS 2³¹-1 test pattern @10.3Gbps, BER ≤1E-12.
5. Internally AC-coupled.
6. Bits 110.3 and bits 118.3 control the locking modes of the internal retimer or CDR, default Value is "1".

Bit 110.3 of A2h	Bit 118.3 of A2h	RX Data Rate	TX Data Rate	Status of RX CDR	Status of TX CDR
High/1	High/1	24.33G/25.78G	24.33G/25.78G	CDR select	CDR select
High/1	Low/0	24.33G/25.78G	9.95G/10.31G	CDR select	CDR bypass
Low/0	High/1	9.95G/10.31G	24.33G/25.78G	CDR bypass	CDR select
Low/0	Low/0	9.95G/10.31G	9.95G/10.31G	CDR bypass	CDR bypass

Digital Diagnostics

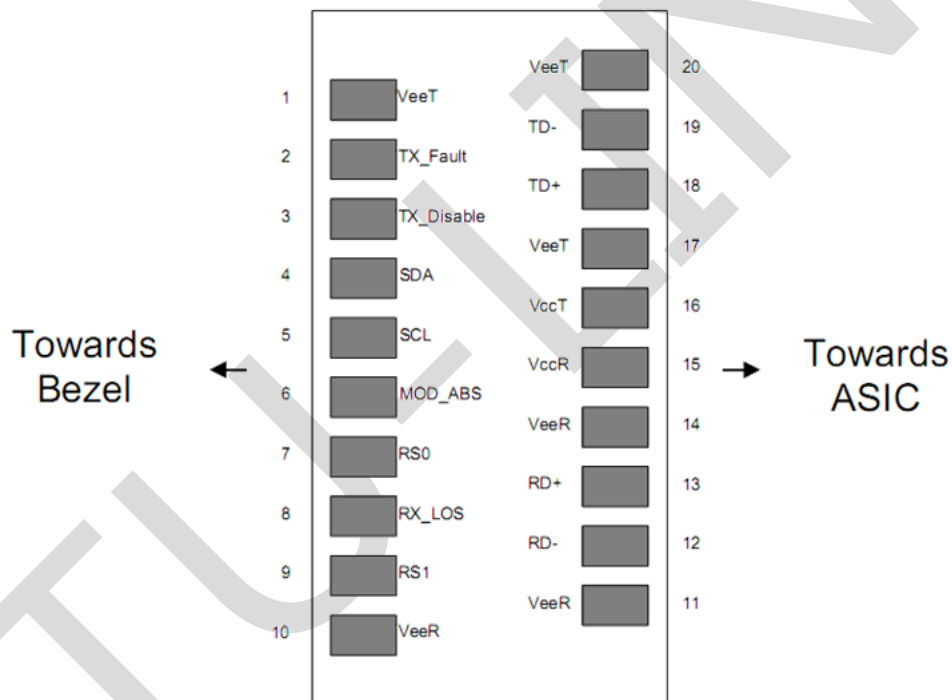
Parameter	Range	Accuracy	Unit	Calibration
Temperature	-40 to +85	±3°C	°C	Internal
Voltage	3.0 to 3.6	±3%	V	Internal
Bias Current	0 to 15	±10%	mA	Internal
TX Power	-8.4.0 to 2.4	±3dB	dBm	Internal
RX Power	-12 to 2.4	±3dB	dBm	Internal

Communication Interface Timing Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Tx Disable Negate Time	t _{on}			2	ms	
Tx Disable Assert Time	t _{off}			100	μs	

Time To Initialize, including Reset of Tx Fault	t_init			300	ms	
Tx Fault Assert Time	t_fault			100	μs	
Tx Disable To Reset	t_reset	10			μs	
LOS Assert Time	t_loss_on			100	μs	
LOS De-assert Time	t_loss_off			100	μs	
Serial ID Clock Rate	f_serial_clock		100	400	KHz	
MOD_DEF (0:2)-High	V _H	2		V _{cc}	V	
MOD_DEF (0:2)-Low	V _L			0.8	V	

Pin Diagram



Pin Definitions

PIN #	Name	Function	Notes
1	V _{EET}	Transmitter Ground	
2	TX_FAULT	Transmitter Fault Indication	Note 1
3	TX_DISABLE	Transmitter Disable	Note 2
4	SDA	SDA Serial Data Signal	
5	SCL	SCL Serial Clock Signal	
6	MOD_ABS	Module Absent. Grounded within the module	
7	RS0	Not Connected	

8	LOS	Loss of Signal	Note 3
9	RS1	Not Connected	
10	V _{EER}	Receiver ground	
11	V _{EER}	Receiver ground	
12	RD-	Inv. Received Data Out	Note 4
13	RD+	Received Data Out	Note 4
14	V _{EER}	Receiver ground	
15	V _{CCR}	Receiver Power Supply	
16	V _{CCT}	Transmitter Power Supply	
17	V _{EET}	Transmitter Ground	
18	TD+	Transmit Data In	Note 5
19	TD-	Inv. Transmit Data In	Note 5
20	V _{EET}	Transmitter Ground	

Notes:

Plug Seq.: Pin engagement sequence during hot plugging.

1. TX Fault is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and V_{cc}+0.3V. Logic 0 indicates normal operation; Logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.

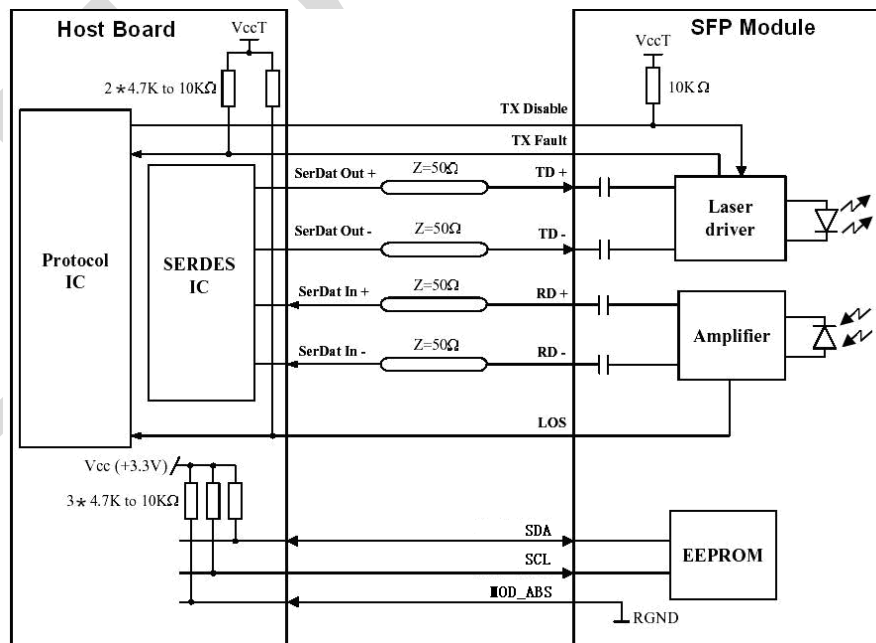
2. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.

3. LOS is open collector output. Should be pulled up with 4.7k~10kΩ on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.

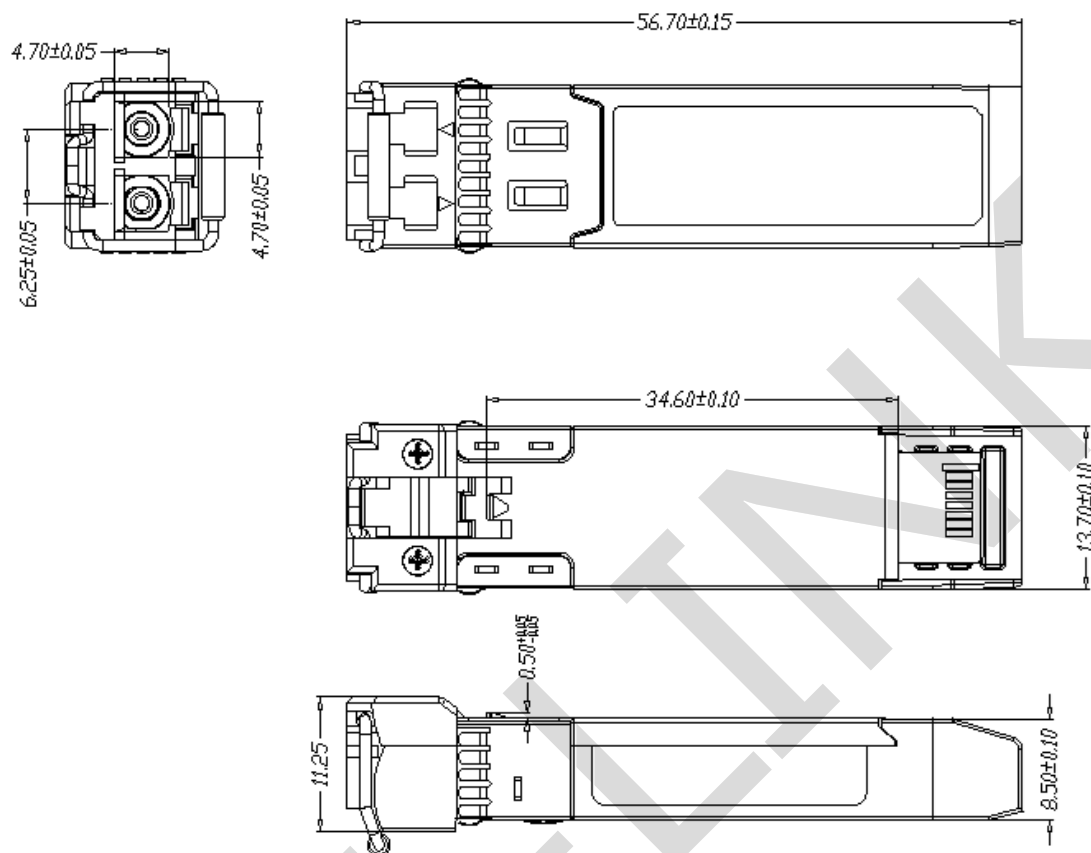
4. RD-/+: These are the differential receiver outputs. They are internally AC-coupled 100 differential lines which should be terminated with 100Ω (differential) at the user SERDES.

5. TD-/+: These are the differential transmitter inputs. They are internally AC-coupled, differential lines with 100Ω differential termination inside the module.

Recommended Interface Circuit



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	May 08, 2018	Preliminary datasheet
2.0	Aug 27, 2024	Format change

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