QSFP28 Series

ETU-LINK

Optical Communication System

QSFP28

EQ2xx10X-3LCD80

100Gb/s QSFP28 ZR4 Transceiver

- Compliant with 100GBASE-ZR4
- Support line rates from 103.125 Gb/s to 111.81 Gb/s OTU4
- LAN WDM EML laser and PIN receiver with SOA
- Up to 80km reach for G.652 SMF
- Hot pluggable 38 pin electrical interface
- QSFP28 MSA compliant
- Duplex LC optical receptacle
- RoHS-10 compliant and lead-free
- Single +3.3V power supply
- Maximum power consumption 6.5W
- Case operating temperature
  Commercial: 0 ~ +70℃
  Extended: -10 ~ +80℃
  Industrial: -40 ~ +85℃

Applications

- 100GBASE-ZR4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Telecom networking

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	Ts	-40	85	℃	
Power Supply Voltage	VCC	-0.3	4.0	V	
Relative Humidity (non-condensation)	RH	15	85	%	
Damage Threshold	THd	6.5		dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TOP	0		70	℃	commercial
		-10		80		extended
		-40		85		Industrial
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			25.78125		Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance (SMF)	D			80	km	1

Notes:

1. Depending on actual fiber loss/km (link distance specified is for fiber insertion loss of 0.35dB/km)

General Description

Designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wireserial inter- face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.

ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

Transceiver Block Diagrams

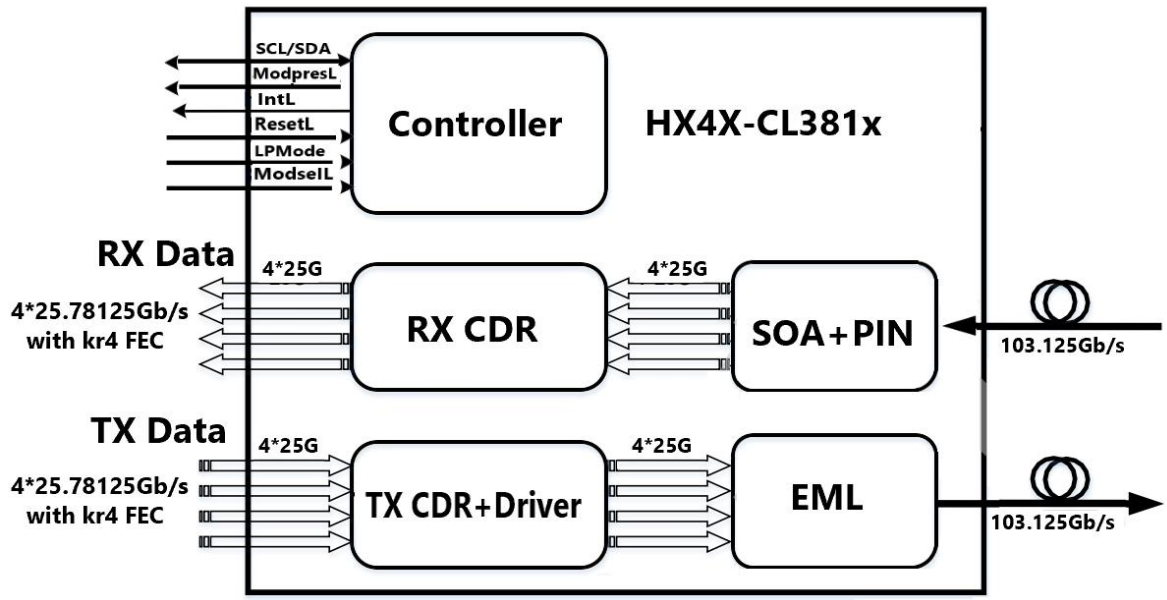


Figure1. Transceiver Block Diagram

ResetL

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode

LPMode: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.

Pin Assignment and Pin Description

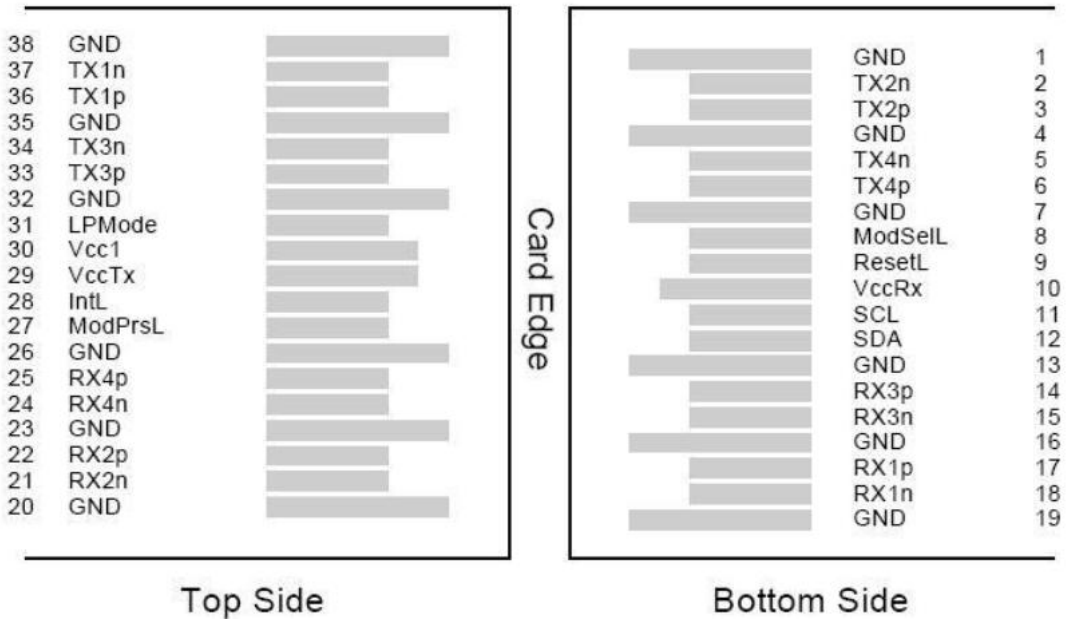


Figure2. Diagram of host board connector block pin numbers and names

Pin	Symbol	Name/Description	Notes
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	

15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc

Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Power Consumption	p			6.5	W	
Supply Current	Icc			1876	mA	
Transmitter (each Lane)						
Overload Differential Voltage pk-pk	TP1a			900	mV	
Common Mode Voltage (Vcm)	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI-28 G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1			See CEI-28 G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a	See CEI-28 G-VSR Section 13.3.11.2.1				
Receiver						
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4			See CEI-28	dB	

				G-VSR Equation 13-19		
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4			See CEI-28 G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10-15 probability (EW15)	TP4	0.57			UI	
Eye Height at 10-15 probability (EH15)	TP4	228			mV	

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.

2. From 250MHz to 30GHz.

Optical Characteristics

The following optical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Lane wavelength（range）	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.09	nm	
Signaling rate, each lane			25.78125		GBd	
Side-mode suppression ratio	SMSR	30				
Total launch power	P_T	8.0		12.5	dBm	

Average launch power, each lane	Pavg	2.0		4.5	dBm	1
OMA, each Lane	P_{OMA}	0.1		4.5	dBm	2
Extinction Ratio	ER	6.0			dB	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			3.6	dB	
Transmitter and Dispersion Penalty, each lane	TDP			2.5	dB	
OMA minus TDP, each lane	OMA-TDP	-0.65			dBm	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Transmitter reflectance	R_T			-12	dB	
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter eye mask {X1, X2,X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Receiver						
Signaling rate, each lane			25.78125		GBd	
Average Receive Power, each Lane		-28		-3.5	dBm	
Receive Power (OMA), each Lane				-3.5	dBm	
Receiver reflectance	SEN1			-26	dBm	for BER = $1x10^{-12}$
Receiver sensitivity Average, each lane	SEN2			-28	dBm	for BER = $5x10^{-5}$
Difference in Receive Power between any Two Lanes (Average and OMA)	Ptx,diff			3.6	dB	
LOS Assert	LOSA	-40			dBm	
LOS Deassert	LOSD			-29	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Conditions of Stress Receiver Sensitivity Test (Note 4)						
Vertical Eye Closure Penalty, each Lane			1.5		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:

1. The minimum average launch power spec is based on ER not exceeding 9.5dB and transmitter OMA higher than 0.1dBm.
2. Even if the TDP < 0.75 dB, the OMA min must exceed the minimum value specified here.

Digital Diagnostic Functions

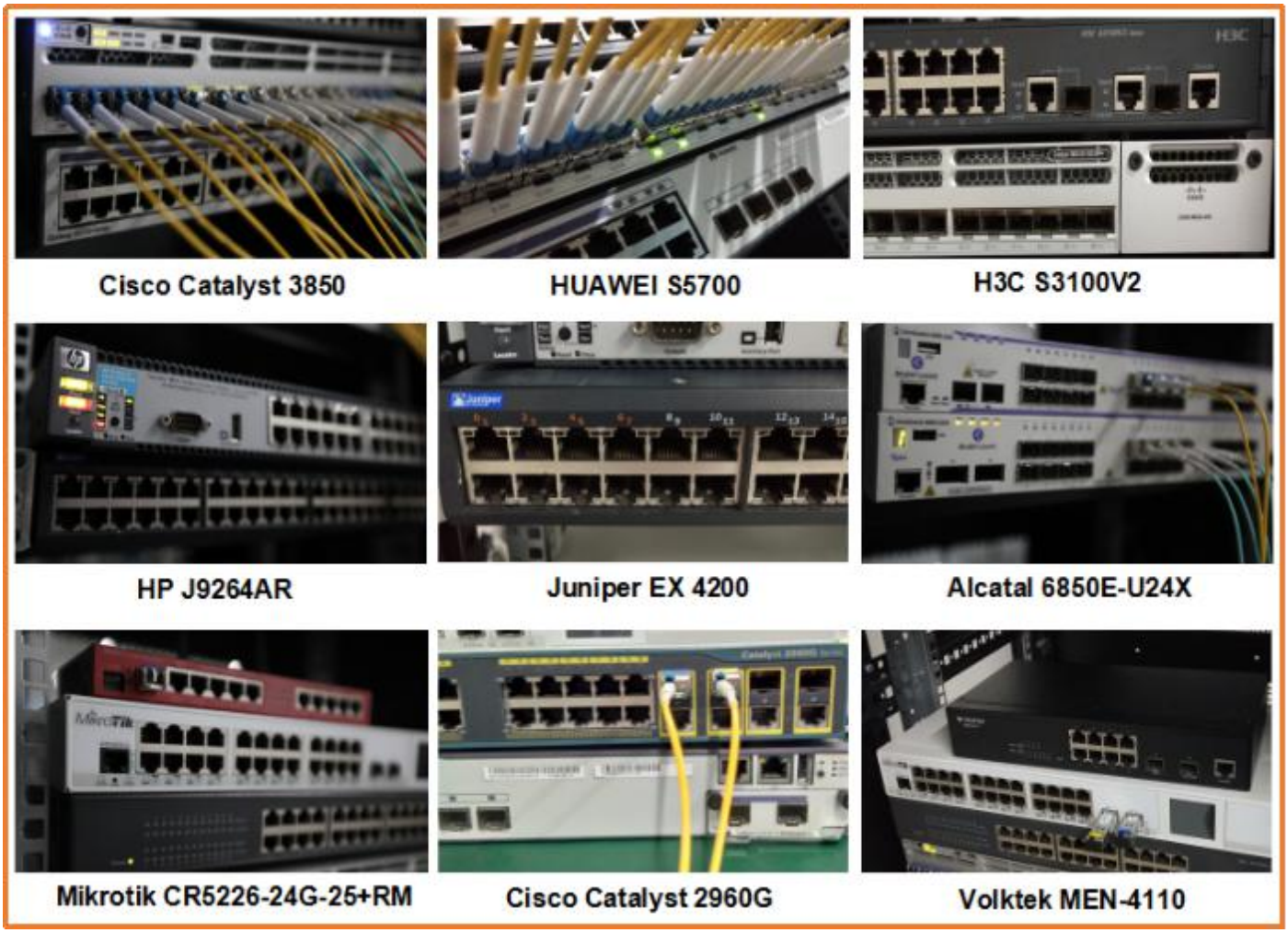
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Max	Unit	Notes
Temperature monitor absolute error	DMI_ Temp	-3	3	ºC	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.15	0.15	V	Full operating range
RX power monitor absolute error	DMI_RX	-3	3	dB	
Bias current monitor	DMI_ bias	-10 %	10%	mA	
TX power monitor absolute error	DMI_TX	-3	3	dB	

Compatibility Test

In order to ensure the product compatibility, our products will be tested on the switch before shipment. Our modules can compatible with many mainstream brand switches, such as Cisco, Juniper, Extreme, Brocade, IBM, H3C, HP, Huawei, D-Link, Mikrotik, ZTE, TP-Link...

Our test equipment: VOLKTEK MEN-4110, HP 2530-8G, CRS226-24G-25+RM, Catalyst 2960G Series, Catalyst 3850 XS 10G SFP+, Catalyst 3750-E Series, HUAWEI S5700Series, H3C S3100V2 Series, Juniper-EX4200, etc.



Cisco Catalyst 3850 | HUAWEI S5700 | H3C S3100V2

HP J9264AR | Juniper EX 4200 | Alcatal 6850E-U24X

Mikrotik CR5226-24G-25+RM | Cisco Catalyst 2960G | Volktek MEN-4110

Product Production Process

Quality Assurance

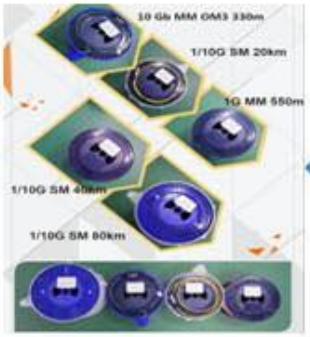
Continuous introduction of new equipment, produced by strict standards, strict quality inspection, to guarantee the high quality standard of each product.

Standardized Production Line

Professional Welding

Assembling

Cleaning end face



Distance Testing

Aging Testing

Product Initial Test

Switch Testing

Product Final Test

Packaging

ETU-Link provides two kinds of packaging, 10pcs/Tray and individual package.

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Tel: +86-755 2328 4603

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Please e-mail us at sales@etulinktechnology.com or call us for assistance.

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