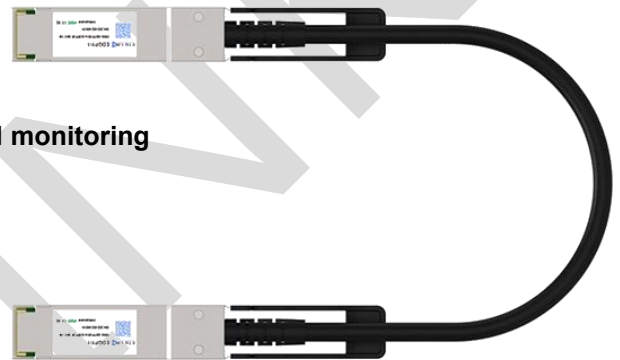


EDQPY-x

100G QSFP28 Copper Cable Assembly

PRODUCT FEATURES

- Compliant with SFF-8636
- Support IEEE802.3Bj(Ethernet)
- I2C based two-wire serial interface for easy control and monitoring
- Hot Pluggable
- Low Crosstalk
- Low power consumption



APPLICATIONS

- 10G/40G /100G Gigabit Ethernet
- Infiniband SDR, DDR, QDR,FDR,EDR
- Servers ,Routers and Switches
- Data Center

Benefits

- Cost-effective copper solution
- Lowest total system power solution
- Lowest total system EMI solution
- Optimized design for Signal Integrity

DESCRIPTIONS

100G QSFP28 passive cable assembly products, based on 4 x25G or 4 x28G structure, the product can well satisfy the next generation 100G switches, servers, routers and other products of application

Requirements. QSFP28 cable adopts optimized design to reduce crosstalk and insertion loss, excellent signal integrity, fully conforms to the next generation 100G Ethernet and Infiniband EDR standards.

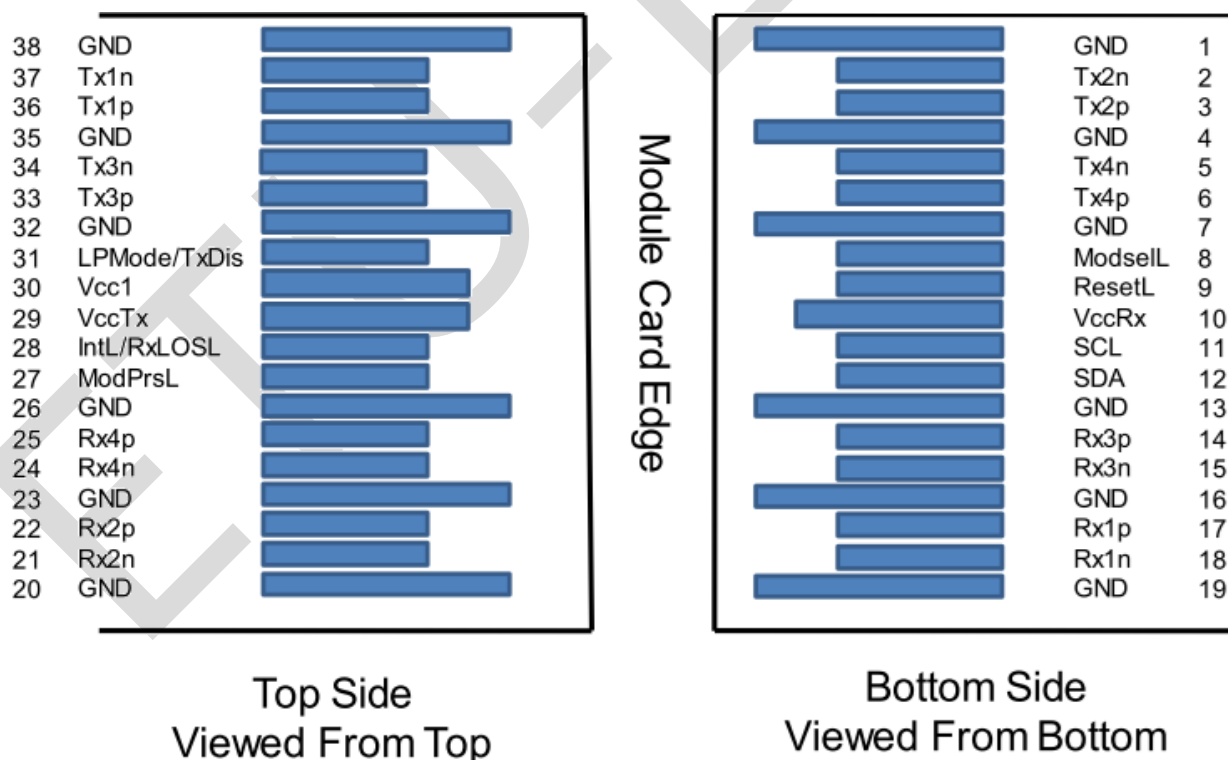
Ordering Information

Part No.	Description
EDQPY-x-30	100G QSFP28 Copper Cable Assembly (DAC) 0~3M 30AWG
EDQPY-x-26	100G QSFP28 Copper Cable Assembly (DAC) 5M 26AWG

Notes:

- where "x" denotes cable length in meters. Examples are as follows:
- x = 1 for 1m,

Pin Diagram



Pin Definitions

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+ 3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/Rx_LOS	Interrupt/Rx_LOS	3	
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode/TxDIS	Low Power Mode/Tx_Disable	3	
32		GND	Ground	1	1

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

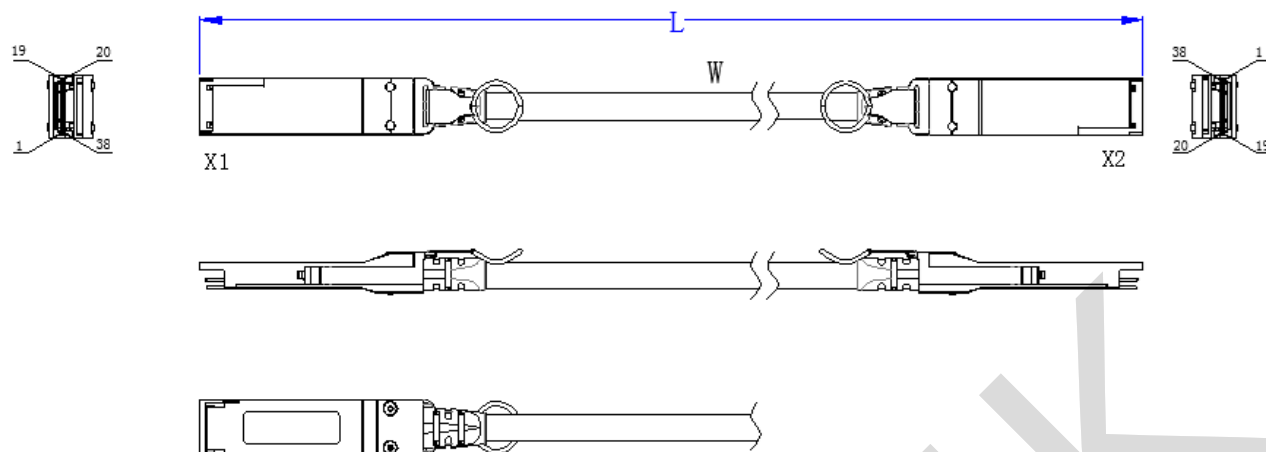
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 Ma

Wiring Diagram

X1	X2	REMARKS	X1	X2	REMARKS
18(RX1-)	37(TX1-)	pair	37(TX1-)	18(RX1-)	pair
17(RX1+)	36(TX1+)		36(TX1+)	17(RX1+)	
15(RX3-)	34(TX3-)	pair	34(TX3-)	15(RX3-)	pair
14(RX3+)	33(TX3+)		33(TX3+)	14(RX3+)	
6 (TX4+)	25(RX4+)	pair	25(RX4+)	6 (TX4+)	pair
5 (TX4-)	24(RX4-)		24(RX4-)	5 (TX4-)	
3 (TX2+)	22(RX2+)	pair	22(RX2+)	3 (TX2+)	pair
2 (TX2-)	21(RX2-)		21(RX2-)	2 (TX2-)	
1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	GND	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	EEPROM point at both ends

Outline drawing



Revision History

Version No.	Date	Description
1.0	February 8, 2021	Preliminary datasheet
2.0	Aug,11,2024	Product upgrades

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