EOP400-SR8

400G OSFP SR8 Optical transceiver for（dual MPO）flat top solution

PRODUCT FEATURES

- **OSFP MSA compliant**
- **8 parallel lanes on 850nm center wavelength**
- **Compliant to IEEE 802.3bs Specification**
- **Up to 100m transmission on multi-mode fiber (MMF) OM3 with FEC**
- **Operating case temperature: 0 to 70℃**
- **8x53.125Gb/s electrical interface (400GAUI-8)**
- **Data Rate 53.125Gbps (PAM4) per channel.**
- **Maximum power consumption 12W**
- **MPO-16 connector**
- **RoHS compliant**

APPLICATIONS

- **Data Center Interconnect**
- **400G Ethernet**
- **Infiniband interconnects**
- **Enterprise networking**

STANDARDS

- **Compliant to OSFP MSA 5.0**
- **Compliant with CMIS 4.0**
- **4x106. 25Gb/s electrical interface (400GAUI-4)**
- **Maximum power consumption 9W**
- **Single +3.3V power supply**

- **Case temperature range: 0 ~ +70□**

- **RoHS 2.0 complaint**

DESCRIPTIONS

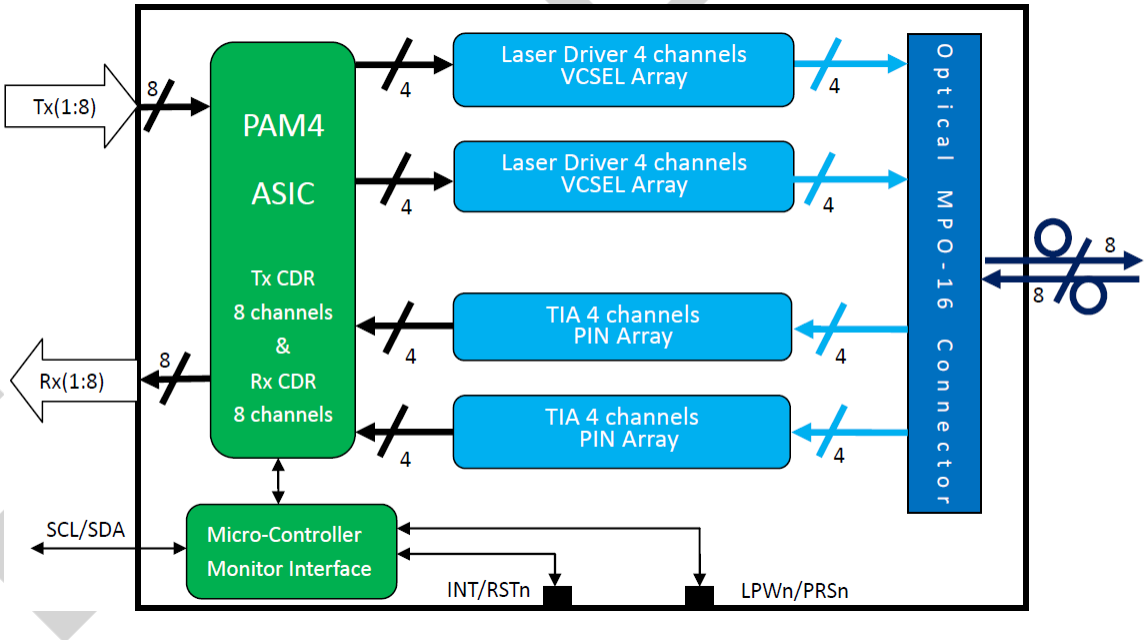
This product is a parallel 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module. It provides increased port density and total system cost savings. The OSFP full-duplex optical module offers 8 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 400Gb/s on 100 meters of OM3 multi-mode fiber.

An optical fiber cable with an MTP/MPO-16 connector can be plugged into the OSFP SR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

The central wavelengths of all the 8 parallel lanes are 850nm. It contains an optical MPO-16 connector for the optical interface and a 60-pin connector for the electrical interface. Host FEC is required to support up to 100m OM3 multi-mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Module Block Diagram



Ordering Information

Part No.	Data Rate(optical)
EOP400-SR8	400G OSFP SR8 Optical transceiver for flat top solution

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings mightcause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	D	0.5		100	m	2

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environmentunless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				12	W	
Supply Current	Icc			3.63	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	

Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode InputVoltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	

Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1.With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2.Meets BER specified in IEEE 802.3bs 120E.1.1.

3.DC common mode voltage generated by the host. Specification includes effects of groundoffset voltage.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
RMS Spectral Width	$\Delta\lambda_{rms}$			0.6	nm	Modulated
Average Launch Power, eachLane	P_{AVG}	-6.5		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), eachLane	P_{OMA}	-4.5		3	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lane		-5.9			dB	
Transmitter and Dispersion Eye Clouser for PAM4, eachLane	TDECQ			4.5	dB	
Extinction Ratio	ER	3			dB	
Optical Return LossTolerance	TOL			12	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-30	dBm	
Encircled Flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				
Receiver						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				

Damage Threshold, eachLane	TH_d	5			dBm	3
Average Receive Power, eachLane		-7.9		4	dBm	4
Receive Power (OMA_{outer}),each Lane				3	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-6.5	dBm	5
Stressed Receiver Sensitivity(OMA_{outer}), each Lane	SRS			-3	dBm	6
Receiver Reflectance	R_R			-12	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane underTest			4		dB	
OMA_{outer} of each AggressorLane			3		dBm	

Notes:

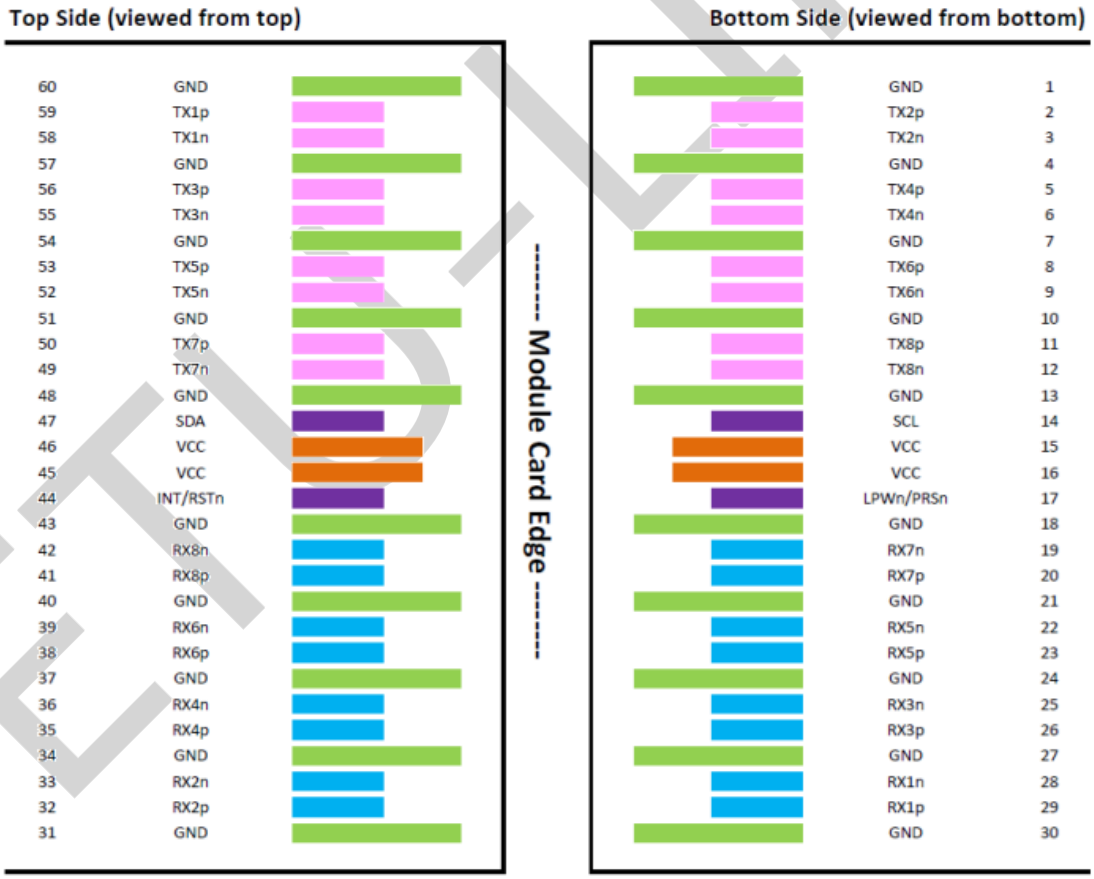
1. Average launch power, each lane (min) is informative and not the principal indicator ofsignal strength. A transmitter with launch power below this value cannot be compliant;however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1 dB , the OMA_{outer} (min) must exceed the minimum value specifiedhere.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an opticalinput signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a valueabove this does not ensure compliance.
5. Receiver Sensitivity OMA_{outer}, each lane (max) is informative and is defined for a BER of$2.4x10^{-4}$.

6. Measured with conformance test signal at receiver input for the BER of $2.4x10^{-4}$.
7. These test conditions are for measuring stressed receiver sensitivity. They are notcharacteristics of the receiver.

Digital Diagnostics

Parameters	Unit	Specification
Temperature Monitor absolute error	°C	± 3
Supply Voltage Monitor absolute error	%	± 5
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

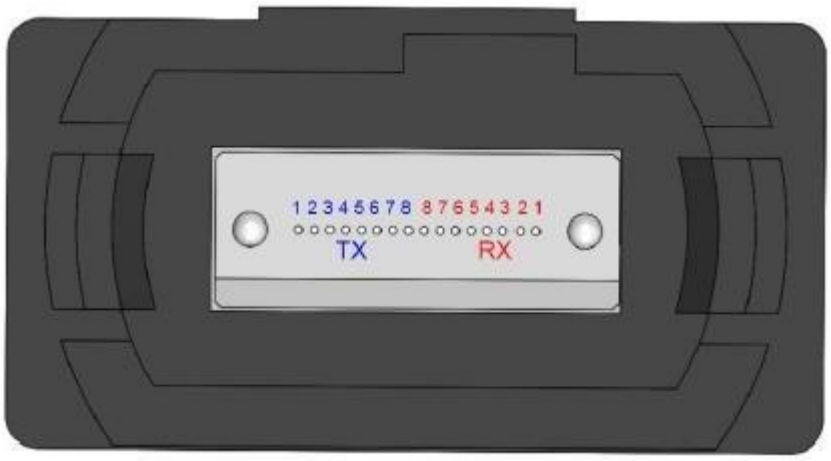
Pin Diagram



Pin Definitions

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1

31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1



Recommended Interface Circuit

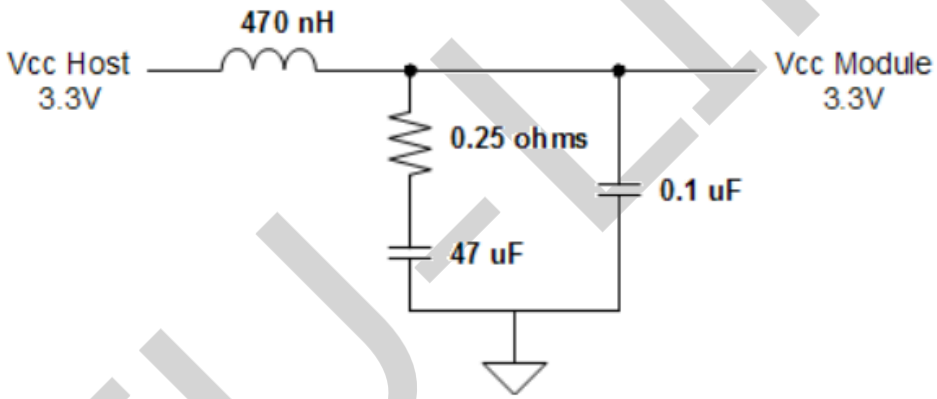
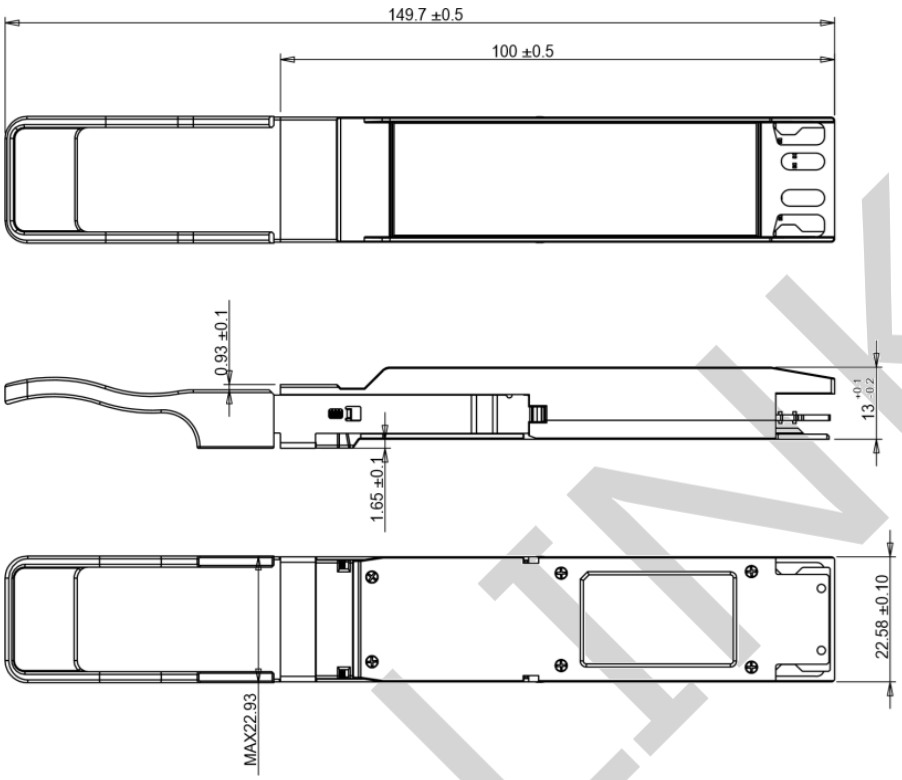


Figure 13-6: Host board power filter circuit

Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2024	Preliminary datasheet
2.0	Oct 05,2024	Format change

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